DESIGN AND CONSTRUCTION OF A DIGITAL WALL CLOCK USING BACK-UP BATTERY

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Abstract

The design and construction of a digital clock is necessary because of the need to measure more accurately the time or period between events. It is aimed at building compactness, improved efficiency, reliability and low noise to signal ratio into the design of digital clock at reduced cost and power consumption rate. A 6V, 4.5AM rechargeable battery is incorporated into the design as an alternative power source in case of power outage. The battery is expected to power the clock for a period of six (6) days of total power outage. The clock was designed using digital counters, BCD - to - seven segment decoders and dividers, digital oscillator and other logic gates.

The clock operates within a nominal supply voltage range of 4.75V to 5.25V, power rating of 7.4W and an ambient temperature range 0"C to 70"C.

Due to the maximum allowable temperature, the clock should not be exposed to continuous heat so as not to affect its accuracy. It should be shielded from direct sunrays so that the LED display can be in good operating condition with accuracy of ±2 seconds / hr. This design finds relevance in various sectors of human life where accurate timing is of paramount interest. Places of relevance includes schools, offices, laboratories, hospital, halls and other public places like sport halls and cinema houses.

Introduction

Time is not paramount but also pivotal to human life, throughout history, time has always intrigued mankind. From the days of judging by the position of the sun, to today's most accurate time piece, the atomic clock, time has. without exception been one of life's constant.

By watching the length of shadows cast by the sun, man realized that the shadow was a more accurate way to tell time, rather than judging by the position of the sun. As time progressed, other means of measuring time evolved and the quest for accuracy began.

The sundial was the earliest and was used well into the eighteen century. It was followed by the clepsydra (water clock) and then the sand glass. The Escarpment was next, then the pendulum clock. The creation of modern case and dial for clock; clock towers with bells to clime different melody everyday (i.e. digital clock) and the atomic clock were the other evolution after the pendulum.

The evolution was mainly due to the desire of man to measure time more accurately and his attempt to overcome the various disadvantages peculiar to each timepiece. These disadvantages include; nature (e.g. during less sunny condition or at night), earth rotation in sundial, water level and water temperature fluctuations in clepsydra e.t.c.

The advent of digital technology commemorated the birth of something revolutionary and unprecedented in the design of timepieces. Due to the definite and accurate measurement it gives, it has stolen the show in contemporary clock designs. Continuous efforts are being made to improve the digital clock's performance both at the design level and at the microscopic level of each semiconductor device that makes up the component parts.

- Source: http://www.emperorclocl.com/info-history.asp.

Materials and Method

Design Procedure of the Power Supply

The importance of power supply in any electronic system can not be overemphasized. Since most electronic circuits and devices require a DC source of power for their operations, the alternating current from the mains has to be transformed, rectified, filtered, and regulated. The schematic diagram of a 5 V power supply used for this design is shown in Figure 1.0.

The Transformation Unit

A 220V/9V a.c step-down transformer was used in the design. The 9V secondary output was selected because of its ability to supply the minimum required voltage to the rectifier and subsequently to the voltage regulator even when there is a reduction in the voltage supplied by the mains.

The Rectification Unit

A full-wave bridge rectifier with diodes D1 to D4 used in this design was chosen with the following ratings to withstand surge from the input supply.

Peak Inverse Voltage, P1V	=1000V
Current rating, If	=1A
Forward Voltage at 1A	=0.9V
Maximum reverse recovery time	=50ns

RS Components (1992)

The diode IN4007 from the data book is preferred for this operation because of its tolerance and ratings.

The d.c voltage (Vd.c) of the full-wave rectifier is

$$Vm = 9 \times \sqrt{2}$$
$$= 12.73V$$

Where Vm is the peak value of the sinusoidal voltage and it is given by:

$$Vm = Vrms \times \sqrt{2}$$

Since a 9 volts a.c is applied to the input of the rectifier then,

$$Vrms = 9V$$

Therefore,

$$Vm = 9 \times \sqrt{2}$$

$$Vdc = \frac{2Vm}{\Pi}$$

$$Vdc = \frac{2 \times 12.73}{\Pi} = 8.0Volts$$

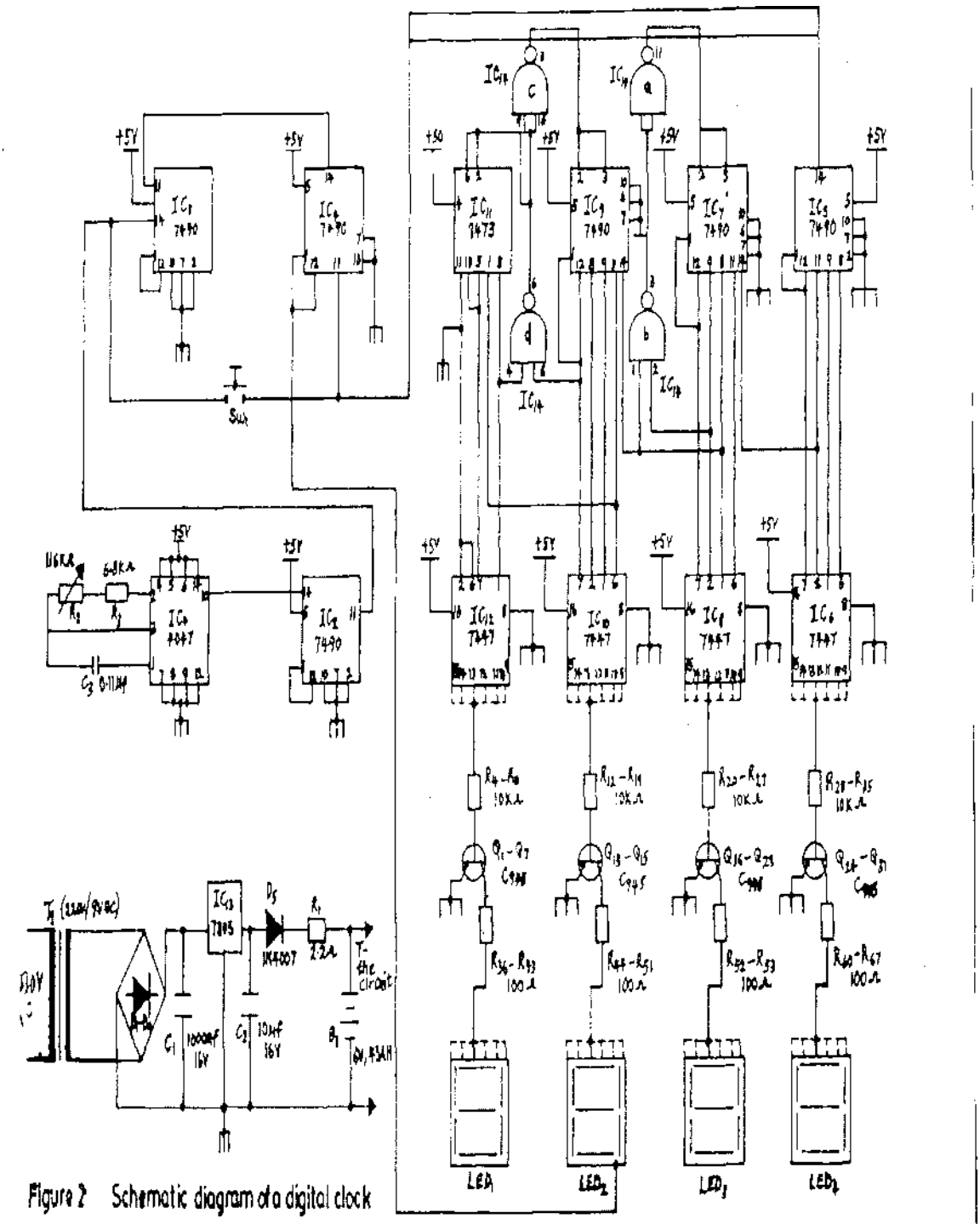

Figure 2 Schematic diagram of a digital clock

The Filtering Unit

A shunt capacitor was used in this design because no external biasing resistor is required in its circuit. A.C ripple which is a form of noise is removed at this stage. The value of the leservoii capacitor used was calculated using the expression:

$$C_1 = \frac{I_{dc}}{2\Pi f V_r}$$

Where V_r = peak-to-peak ripple magnitude, f = frequency

(RYDER, 1987)

But $$Vdc = Vm - \frac{Vr}{2}$$

Substituting $V_{dc} = 8V$ and $V_m = 12.73$ V

$V_r = (12.73 - 8) \times 2 = 9.46$ V

Substituting $V_r = 9.46$ V, $I_{dc} = 1A$

$f = 50Hz$

$$C_1 = \frac{1}{2 \times 3.14 \times 9.46 \times 50} = 337\mu F$$

Preferred value of C_1 =1000μF

The Regulating Unit

IC_{13} (LM 7805) was used in this design because of the following characteristics:

Input Voltage range	= (7 – 25) V
Percentage load regulation	= 0.2
Percentage line regulation	= 0.2
Output resistance	= 30mΩ
Output noise voltage at 1 KHz (typical)	= 40μV
Output current	= 750 mA
Output voltage	= 5V load regulation percentage
Maximum current	= 1 A

- **(RS Components, 1992)**

The regulator is preferred because it makes the power supply unit's circuitry less complex an it adds to the homogeneity of integrated circuit usage in the digital clock circuit.

The Pulse Generating Unit

The IC_1 (4047) has the following characteristic:

Supply voltage range	= 3 V to 18V d.c
Current (typical)	= 12 mA
Input current	= 1.6 mA /input
Propagation delay time (typical)	= 40ns to 175ns
Fan out	= 10
Power dissipation / gate (typical)	= 2.7nW to 1 70pW
Temperature range	= 40"C to125°C

The 1Ci(4047) has a very good external noise immunity, all its outputs are buffered, it has double diode protection on all inputs and its capacity of driving two low-power TTL loads/one low- power schottky TTL load over the rated temperature. The pulse-generating unit and the pin out of IC|(4047) is shown in Figure 1.0.

(Cook, 1998)

The clock frequency is obtained by the expression given below

$$f = \frac{1}{4.44RC}$$

- (Horowitz and Hill, 1995)

Where, R =R2 + R3 and C = C2

R3=6.8KΩ and R2 = 116KΩ

Therefore, R =122.8KΩ, C = 0.11μF

$$f = \frac{1}{4.44 \times 122.8 \times 10^{3} \times 0.11 \times 10^{-6}} = 16.67 Hz$$

Hence, the frequency of operation of the pulse-generating unit is 16.67Hz

The Frequency Division / Counting Unit

The arrangement of 4 J-K flip-flops with associated NAND gates can be used to implement a decade counter. It is however usually more convenient to employ a decade counter (e.g. 7490). Figure 2.0 shows a 7490 configured for a decade counting. The 1C is arranged internally in two sections divide by 2 and divided by 5. The master clock pulse is applied to the input of the divide by 2 (pin 4) which divide the pulse by two and the output Q_0 (pin2) is then connected to the divide by 5 clock input (pin 1). The corresponding output Q_0, Qi, Q_2 and Q_3 gives the BCD equivalent of the count. To set a 9 (1001), pins 6 and 7 are ground. Similarly, a reset 0 (0000), pins 2 and 3 are also grounded. T his prevents the output from arbitrarily getting to 9 or resetting to 0.

Figure 2.0 shows a 7490 connected as a MOD-10 counter. The output Q_2 (pin I 1) provides the divide by 10 output. This will act as the clock pulse for the counter.IC_2, IC_2, $IC_{.t}$. IC_5 and IC_9 are examples of 7490 connected as a divide by 10 counters.

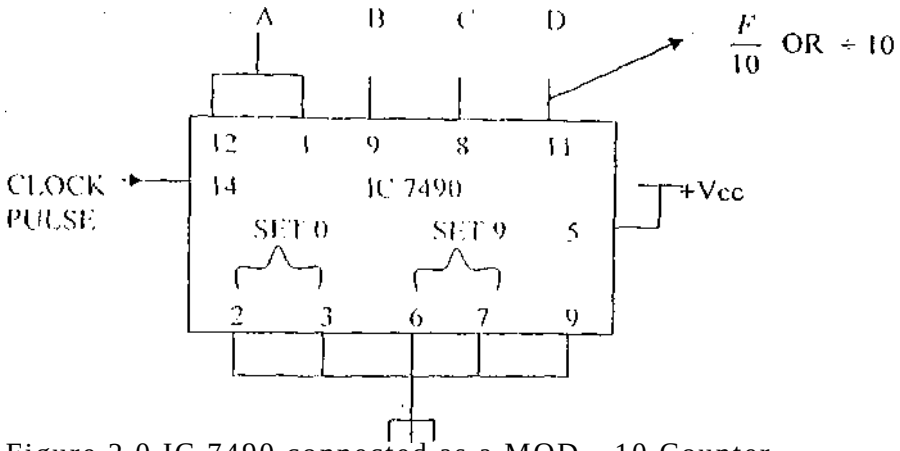

Figure 2.0 IC 7490 connected as a MOD - 10 Counter

MOD - 6 Counter

The 7490 IC could be configured as a MOD - 6 counter that counts from 0 to 5 and reset back to 0. This can be achieved by first connecting pin 12 ($Q_{„}$) to the clock input of the divide by 5 counter (pin I). The set 9 pins are grounded as shown in figure 3

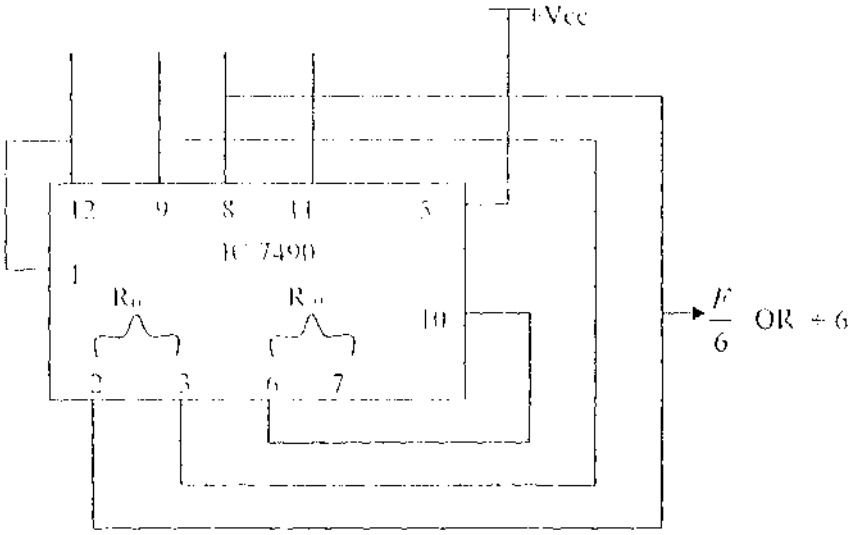

Figure 3.0 IC 7490 Connected as MOD - 6 Counter

To interrupt the count alter the sixth count, the reset 0 pin is connected to pin 5, 8 and 9 which are HIGH f at the seventh count. The HIGH outputs will force the counter to reset zero and the cycle repeals. The MOD -6 output is obtained from pin 8 of the 1C.

MOD - 2 Counter

ICu is a MOD - 2 counter. The 7473 IC is a **DUAL J-K** flip-flop with 14 pins. One of the flip-flops was used to generate the tens of the hour stage. Pin4 of FF_1 was connected to the voltage
supply while the bubbled input pin I was connected to the output of IC_9 (7490). The Q output of the flip-flop was used however instead of the 0 output.

The Decoding Unit

A decoder is a digital circuit that responds to a particular coded signal while rejecting others. It converts binary information from a coded input counter output to maximum of 2" unique outputs. Basically, a decoder circuit is a combinational logic circuit made from (AND and NAND) gates and INVERTERS.

$IC_{(}$„ IC_S, ICi<) and IC_{12}. from the complete circuit diagram (i.e. Figure 1) are 7447 and are used as a decoder/ driver which means that the output has an open collector which requires a pull-up resistor. The pin-out of 7447 is shown in Figure 4 with four BCD inputs and seven outputs hence thee name BCD-to- seven segment decoder.

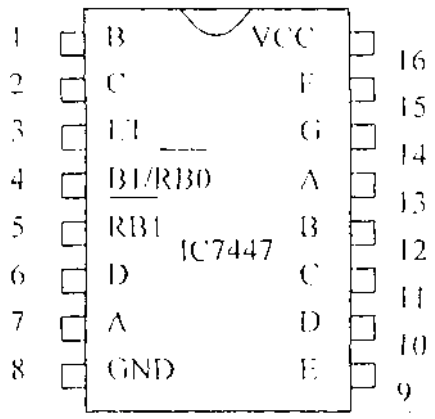

Figure 4 Pin-out of 1C 7447 (decoder)

fhe outputs labelled A, B, C, D, E, F and G are used to drive the arranged LEDs. These 74xx !Cs belong to the TTL (Transistor-Transistor Logic) family with the following characteristics:

Temperature range	=0°C to 70"C
Maximum sw itching frequency	(MHz) =45 MHz
Fan-out	=2
Power dissipation / Gate	=2mW
Propagation delay /Gate	=8ns
Typical supply voltage	=+5V
Typical Input signal frequency	=15 to 120MHz

They' also have good external noise immunity and a medium-high internal generated noise. The active outputs are at logic LOW and sinks current of up to 30VcLc

The Transistor Driver and Display

The characteristics of the transistor used are given below:

Max. Collector current, l.C	=200mA
Max. Collector-Emitter voltage, $Vce_{()}$	=30V
Max. Collector- Base voltage, Vcb_0	=45V
Current gain life (typical)	=250
Max.Power, Pc	=300mW

(Tooley, 1993)

Number of LEDs per segment	= 11
Current drawn per segment	=7mA
Therefore, the total current per segment	=77
Voltage drop across the LED	=2.2V
Vce (typical)	=0.9
Therefore, voltage drop across the resistor	=12-(2.2 + 0.9)
Voltage drop across the resistor	=8.9V

Since the total current through the collector circuit is 77mA the value rate of the resistor is obtained as follows; R = V/i

$$R = \frac{8.9}{0.077} = 11.58 \text{ Ohms}$$

The preferred value used is 100 Ohms.
The power in the resistor is $I^3R = (77x\ 10^{-3})^2 x100$

The Display Unit

There are basically two types, the Indicator tubes and the seven segments. The seven-segment display was used and configured using the common- anode configuration because of the 7447used.

The LED used in this design is of the Ga A/As Ultra-Bright type. It is preferred to all other types because of its characteristics listed below.

Colour	=Red (Intensity as 29mA (typical) – l000mcd)
Po (Max)	=100mW
V_r(type)	=2.5V
If (Max)	=50mA
V_R (Max)	IV
Peak wavelength	=660nm
View ing angle	=10"

(RS Components; 1992)

Principle of Operation of the Digital Wall Clock

The mains of the power supply (i.e. 220Vac / 50Hz) were taken from A.C source to a step- down transformer, T1 (i.e. 220Vac / 9Vac) (see Figure 1). The output of the transformer, T1 was fed to a bridge rectifier.

Due to the arrangement of the diodes in the full-wave bridge rectifier, current flows throughout the cycle of the input, 'flic rectifier wave is filtered by the capacitor C t (1 00JLI f, 16V). The shunt capacitor filter is used because there is no external biasing resistor. This ripple- free wave is fed to the voltage regulator LM7805 to produce a constant positive 5V-dc supply as shown in the complete circuit diagram. (Fig 1)

Battery, B| (6V, 4.5AM) is charged by the regulated voltage and it supplies the required voltage in case of power outage.IC (4047) produces the clock frequency, which is a function of the value of the capacitor, C| and the sum of the resistors R_2 and IG is fed into IC2 (7490). The output frequency (16.6711/,) from the oscillator, 1C|, is converted to 16.667PPM. 0.1667PPM, and 0.01667PPM respectively by the operation of MOD- l0counters $1C_2$, IC_3 and IC_4

Since the minute stage of the clock uses a decade counter and a MOD-6 counter, the 1PPM fed into the stage through pin 14 of IC_5 (7490) registers every 60 seconds of the pulse as a minute. The output of the minute counters are connected to the decoders (IC\, and IC_8 -7447) which decodes the clock's signal and displays the decimal equivalent of the time on the seven segment display. The ripple- carry -out of the minutes counter is used to clock KY (7490) that is the unit of the hour counter that counts from 0 to 9. The hour counting stage comprising ICY (7473) and IC_9 (7490) performs the operation of counting from 0 to 4 and resets IC_9 (7490) whenever count 3 is reached. The resetting is done by QB of lC_{11} (7473) must be HIGH.

The HIGH outputs are then connected to a NAND gate (pin 4 and pin 5) of $IC_{!4}$ (7400) so that a LOW output is used to reset the flip-flop (IC_{11}) so that its output (pin 6) is forced LOW.

Similarly, the low output obtained from pin 6 of IC_{14} (7400) is inverted by NAND gate (IC_{14}) to obtain a HIGH output, which also reset the unit of hour counter (IC_9 -7400).

Since IG; (7490) is a decade counter, it counts from 0 to 9 and then resets back to zero. This also-will cause the flip-flop (IC_{11} -7473) to toggle from 0 to 1 and then to two. This counter registers the hour from the first to the twelfth hour as displayed by the seven-segment display. The NAND gates (IC14 c and d) prevents the hour count from advancing the count to 13 by

causing the counter to toggle to zero during the thirteenth count, flip-flop (IC_{11}-7473) is cleared and the decade counter is presetted to 0001 BCD.

The BCD output from the minutes and hour counter are decoded by BCD to seven segment decoders, IC12, 1C 10, 1C8, and IC6. These seven-segment codes drive the common-anode display via the transistor drivers to register the time.

Clock Setting

l he clock pulse from the output of IC_{11} (4047) -pin 10 is used to clock the divide-by-one thousand (i.e. MOD- 1000) counter and to set the time. To set the time, the SET switch swl (a normally- open switch) is pressed so as to feed a high frequency pulse to the minutes and the hour counters to advance the counting operation. The period obtained from this particular frequency is in the order of milliseconds thus making the toggling operation of the minutes and hour stage faster. Releasing the SET switch changes the clock from set mode to normal counting resumes.

(Cook, 1998)

Results and Discussion

After the construction of the digital clock, tests were carried at different stages of the circuit to measure the magnitude of the voltage at such points. The output of the step-down transformer, Tl, was 9V a.c corresponding with the expected 9V a.c output.

Also, the output of the voltage (LM 7805) was also measured. This was necessary because the circuit was designed to operate at 5V dc supply. The result of the test revealed that exactly 5V dc was present at the output of the monolithic regulator.

The magnitude of the logic LOW and logic HIGH measured at the input of the counters (1C 7490) was 0.2V d.c and 4.85V dc respectively. When compared with expected result, it was observed that there was a loss of about 0.2V. This was attributed to the voltage drop across the components inside the integrated circuit. The loss however, did not affect the operation of the counters. For a TTL the expected magnitude of the logic LOW is 0V (ideal) while that of logic HIGH is 5 V (ideal).

The result obtained at the decoder input (1C 7447) dc was compared with the expected result from a TTL; it was observed that the loss of about 0.2V dc was due to the further drop of voltage across the components inside the ICs.

Transistors (A 101 5) between the decoders and seven segment display read a VCC of 12V, a base voltage of 0.2V dc for the logic LOW and 4.75 V dc for logic HIGH and a voltage of 2.2 V dc across the LEDs. These losses were varied slightly when compared with the expected result. These losses were attributed to the differences between the calculated results and the preferred values of components.

Digital circuits are very sensitive to the magnitude of voltage present at their inputs. If priority is not given to this, there is bound to be errors since logic levels are alternated readily. Therefore, it was generally observed that the magnitude of the voltage necessary to ensure the smooth operation of the circuit was not exceeded.

Furthermore, the frequency output of the digital oscillator was measured using the frequence' meter. The output of IC1 (4047) was 16.67Hz. This was the exact value calculated. The output of 1C2. IC'3 and 1C4 (7490) were 1,667Hz, 0.16671 Iz and 0.01667Hz respectively.

However, when the clock frequency was fed into the digital clock circuit, and the time set, it was discover that after every one hour the clock was two (2) seconds faster than other clocks. This implies that after 24 hours, the clock will be 48 seconds faster. This test showed that the values of resistors and capacitor used at the pulse generating stage to determine to determine the clock frequency was not accurate enough.

Conclusion and Recommendations

The design and construction of Digital Wall Clock was successful. Tire clock gives accurate time of the day.

From the cost analysis of the project, it was discovered that the digital wall clock (Using Battery back-up) is more economical than the imported ones. The components were found to be available in the market. Cheap cost of production and maintenance is an impetus for mass production at affordable price(s).

A back-up Battery with better capacity can also be used in subsequent work to increase the time of operation of the clock during periods of electric power outages.

The design could be more compact if a smaller but capable battery is used. This will make the casing more compact thus adding more elegance to the design.

The digital wall clock can be used in houses, industries, factories, banks, trains, e.t.c and all places that requiring the accurate time of the day.

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